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09/842,333	04/25/2001	Brian William Hughes	10004547-1	7542

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	2

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/842,333	Applicant(s) HUGHES ET AL.	
	Examiner Esaw T Abraham	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1 to 19** are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims **1 to 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshiaki et al. (U.S. PN: 5,555,212).

As per claims **1 and 9,** Toshiaki et al. teach a method and apparatus for redundancy word line replacement in a semiconductor device involves generating a control signal which causes the data on the data lines to be flipped when the bit pattern of the memory cells coupled to a redundant word line are complementary to the bit pattern of the memory cells of a defective word line which is being replaced by the redundant word line (see col. 1, lines 7-11). Further,

Toshiaki et al. teach a method for testing a semiconductor memory device including normal memory cells and redundant memory cells wherein the normal memory cells are connected to normal word lines and the redundant memory cells are connected to redundant word lines and further the method comprising the steps of detecting (error locating) a defective memory cell in a normal memory cell array, inhibiting a normal word line connected to said detected defective memory cell from being accessed, and replacing the defective memory cell with a redundant memory cell connected to a redundant word line (see claim 1 and claim 30). Furthermore, Toshiaki et al. teach a semiconductor device memory cells arranged in rows and columns, the memory cells including normal memory cells and redundant memory cells for replacing defective ones of the normal memory cells and further a data flip circuit selectively flips data signals on first and second I/O lines (see col. 4, lines 3-19). Toshiaki et al. **do not explicitly** teach repairing a group of N elements of the plurality of elements wherein N is greater than 1 and the group of N elements includes the element. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made to design and define repairing group of N (numbers) elements (rows and columns) to a specified number (for example; from N value to N++) is required in any memory repairing systems depending the system's requirement. **Accordingly,** it would have been obvious to one ordinary skill in the art to design or pre-determine the number of repairing memory elements to any specified number in order to obtain a desired value.

As per claims **2 and 10,** Toshiaki et al. teach all the subject matter claimed in claims 1 and 9 including the step of inhibiting a normal word line connected to said detected defective

memory cell from being accessed, and replacing the defective memory cell with a redundant memory cell connected to a redundant word line (see claim 30).

As per claims **3 and 11,** Toshiaki et al. teach all the subject matter claimed in claims 1 and 9 including a method and apparatus for replacing defective memory cells in a semiconductor memory device using redundant memory cells (see col. 1, lines 8-11).

As per claim **4,** Toshiaki et al. teach all the subject matter claimed in claim 1 including a semiconductor device includes memory cells arranged in rows and columns, the memory cells including normal memory cells and redundant memory cells for replacing defective ones of the normal memory cells (see col. 4, lines 3-19).

As per claim **5,** Toshiaki et al. teach all the subject matter claimed in claims 1 and 4 including Toshiaki et al. teach a semiconductor device includes memory cells arranged in rows and columns, the memory cells including normal memory cells and redundant memory cells for replacing defective ones of the normal memory cells (see col. 4, lines 3-19). Toshiaki et al. **do not teach** initializing a row register or a column register is before or prior to the step of testing. **However,** the practice of initialization before testing is known in the art since row registers or column registers must first initialized (setting addresses or contents of storage to zero or other starting values at the beginning of, or at the prescribed points in) and by virtue of the fact row/column registers must be initialized or configured before testing any storage sub elements in a the memory system. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to initialize registers before testing. **This modification** would have been obvious because a person having ordinary skill in the art would

have been motivated to do so because initializing or configuring registers before testing are well known futures of memory testing systems.

As per claims **6, 7, 12 and 14,** Toshiaki et al. teach all the subject matter claimed in claims 1 and 4, including inhibiting a normal word line connected to said detected defective memory cell from being accessed, and replacing said defective memory cell with a redundant memory cell connected to a redundant word line, determining whether an input row address is identical to a stored row address, the stored address indicating the normal word line connected to said defective memory cell, determining whether data stored in a memory cell to be accessed by the input row address is identical to data stored in a replaced normal memory cell when the input row address is identical to the stored row address, flipping data in order to write the data in redundant memory cell when the input row address is different from the stored row address and reading the data written in said redundant memory cell to flip the data (see claim 30).

As per claims **8 and 13,** Toshiaki et al. teach all the subject matter claimed in claims 1, 9 and 4. Toshiaki et al. **do not teach** incrementing column and row register. **However**, the step of incrementing row or column registers is known in the computer art because in a computer, a register is one of a small set of data holding places that are part of a computer processor wherein the data are commonly incremented or decremented for further computations. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to increment row and column registers. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the steps of incrementing row or column registers are well known futures of computer processors.

3. Claims 15-**19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (U.S. PN: 5,568,408) in view of Nagai et al. (U.S. PN: 6,246,616).

As per claim **15,** Maeda teach an automatic repair data editing system is associated with a repairing system for rescuing defective semiconductor memories fabricated on semiconductor wafers from rejection further the system edits repair data that is partially duplicated due to a trouble in the repairing system, and allows the repairing system to automatically carry out a repair work on the defective semiconductor memories (abstract). Further, the automatic repair data editing system comprising a repair data producing means (repair logic) for performing test sequence for each semiconductor integrated circuit fabricated on semiconductor wafers and for producing pieces of repair data used for rescuing defective semiconductor integrated circuits, an editing means (compare circuitry) for comparing pieces of second identity data with pieces of first identity data to determine if the pieces of repair data contain duplicate pieces of repair data and the editing means further deleting the duplicate pieces from said pieces of repair data (claim 1). Maeda **does not explicitly teach** an inhibit circuitry for that prevents the repair logic from operating on the memory elements. **However,** Nagai et al. in analogous art teach a redundancy file memory having normal memory area and redundancy memory area for recording a replacing information for the cell accessed in the normal memory area, and outputting a signal of the replacing information and a selecting circuit for inhibiting selection of the normal memory area and permitting selection of the redundancy memory area, in response to the signal of the replacing information corresponding to the defective cell (see col. 3, lines 10-22). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention

was made to modify the editing system with the Nagai's a selection circuit for inhibiting memory area. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to increase the probability of relieving a redundancy cell (see col. 2, lines 40-43). Further, Toshiaki et al. **do not explicitly** teach repairing a group of N elements of the plurality of elements wherein N is greater than 1 and the group of N elements includes the element. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made to design and define repairing group of N (numbers) elements (rows and columns) to a specified number (for example; from N value to N++) is required in any memory repairing systems depending the system's requirement. **Accordingly,** it would have been obvious to one ordinary skill in the art to design or pre-determine the number of repairing memory elements to any specified number in order to obtain a desired value.

As per claims **16-19,** Maeda in view of Nagai et al. teach all the subject matter claimed in claim 15 including Nagai et al. teach a selecting circuit for inhibiting selection of the normal memory area and permitting selection of the redundancy memory area, in response to the signal of the replacing information corresponding to the defective cell (see col. 3, lines 10-22). Further, Nagai et al. teach the replacing information is read out from the redundancy file memory corresponding to the driven word line when selecting and driving the word line, the signal of replacing information is used to inhibit to select the normal memory area and to permit to select the redundancy memory area and furthermore, even if only one redundancy column is provided in the redundancy memory area, it becomes possible to relieve (clears) the defective cell generated in plural columns in the normal memory area (see col. 7, last paragraph).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,717,696 Gabillard et al.

US PN: 6,310,807 Ooishi et al.

US PN: 6,341,090 Hiraki et al.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner